Advanced NAND Flash Memory Single-Chip Storage Solution

The growing complexity of flash memory management algorithms has made controller designs complex and has impacted the performance and the diversity of NAND devices that a single controller can support. As the complexity of the controller design increases, there comes a point where hardware acceleration is necessary. We see this trend for partial FTL (Flash Translation Layer) layers, addressing and wear leveling, and command queuing.

At the same time, algorithms and flash device characteristics constantly change through the life of the controller. But data center managers expect the controller to constantly make design tradeoffs in order to improve in-system performance. These changes are also impacted by the traffic patterns of the application. The challenge is to provide hardware-accelerated algorithms that can change frequently in the field.

The Context

Solid-state storage based on NAND flash technology has become an important new lever for improving data-center performance and predictability. But the solid-state drives also present cost and predictability issues of their own. Surprisingly, these issues can be addressed through design of the flash memory controller.

The NAND array has become the dominating factor for the cost of the drive. Increasing the life expectancy of the NAND array obviously reduces the total cost of ownership of the system. Also, the ability to reconfigure the controller to implement improved algorithms or to adapt to a new generation of flash chips extends the system life.

Performance predictability and throughput are key concerns for data-center managers. Throughput must be predictable not only from transaction to transaction, but throughout the life of the drive. With conventional controllers, however, performance drops off with age. There are many reasons for this tail latency: block reclaim, large writes, and multi cycle error correction, for example. Conventional controllers cannot overcome these problems.

Altera worked with two partners, Mobiveil and NVMDurance, to bring together all the significant components of a new kind of flash memory controller on a single FPGA SoC chip.

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The Design

The approach taken for this design is very different from current controllers. Where today's controllers rely on error correction and DSP-based functions for data recovery, our process is to manage the NAND throughout its life, constantly adjusting the controller to minimize bit error rates and to reduce retries or re-read operations and to reduce the number of iterations for the LDPC (Low Density Parity Check) error correction.

The top level of the SSD controller has 4 major components:

• a host interface

• SSD processing and control

• a local processor subsystem

• the flash interfaces.
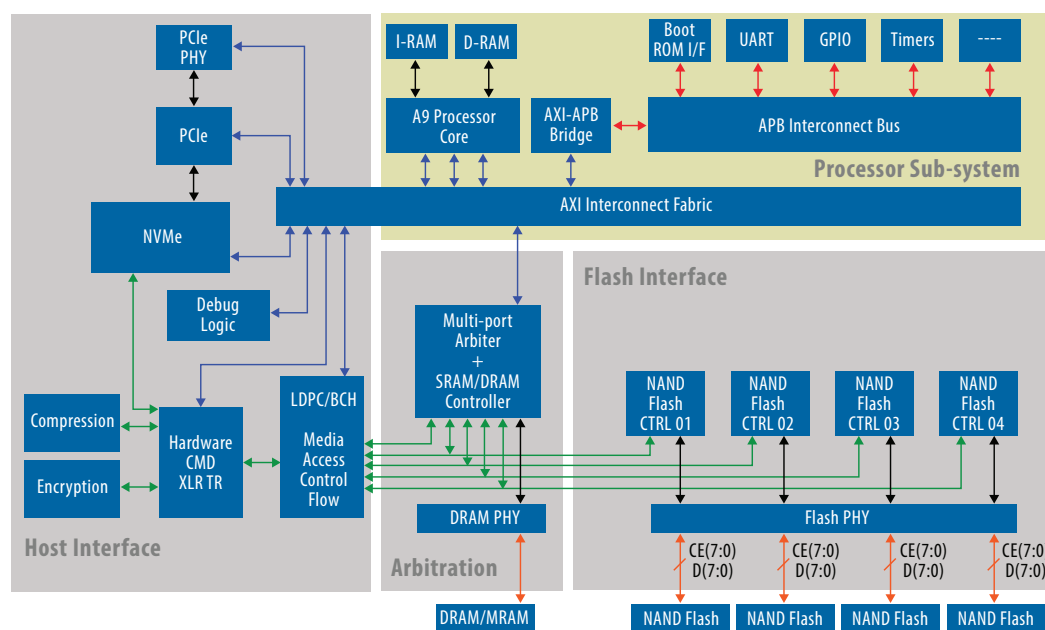
The host interface includes the PCIe PHY, the PCIe endpoint, and the NVMe hardware module. These modules take care of the PCI and NVM protocols and convert them into a disk protocol in the form of command, data, and status transactions.
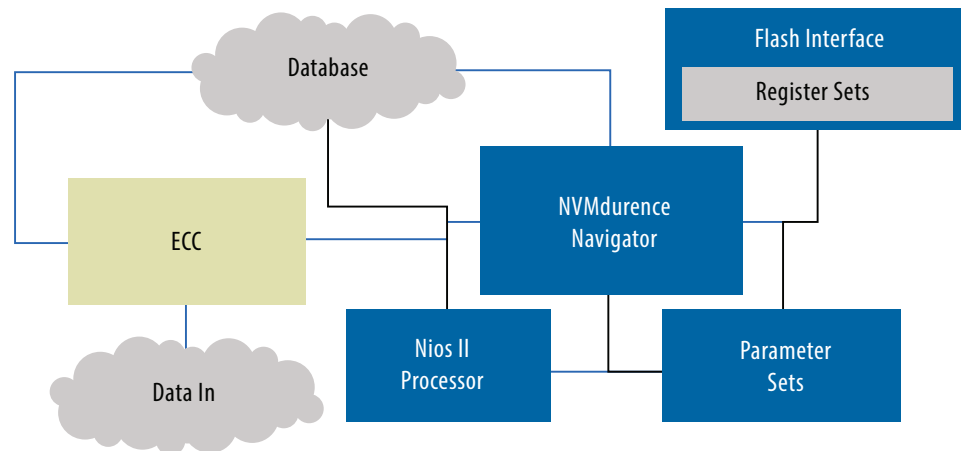
The SSD processing and control block handles the processing of the read/write commands and provides the FTL function in hardware along with compression and encryption in the data path. The media access module allows the scatter and gather functions to write and read to the Flash controllers. The SSD block also includes a DDR SDRAM controller for temporary storage of non-host data.

The flash interface group is composed of a number of flash interfaces for independent access to the flash devices.

The local ARM processor subsystem is used for several key functions in the design. The subsystem peripherals are used for programing, RTC, UART, and other controllers. The processor firmware is responsible for initializing all the hardware, processing and reporting system errors and for the processing of all commands that the hardware command accelerator cannot process.

Theory of Operation

In many respects, the controller operates as a conventional SSD controller. But there are two unique hardware-assisted functions that change the game. The first, Pathfinder, is a set of algorithms that can completely characterize NAND devices from the beginning to the end of life and devise an adaptive set of control register values uniquely suited to your application's requirement for this part number. The second, Navigator, is a lightweight set of controller-side library routines that manages each block in each LUN in an SSD using the data gathered during the Pathfinder characterisation run.

Database

Flash Interface

Register Sets

ECC

NVMdurence Navigator

Data In

Nios II Processor

Parameter Sets

Unlike other methods, Navigator intervenes before the data has been corrupted by the use of inappropriate programming conditions. As such, the process is completely complementary to all other ECC/Write Amplification reducing techniques. Navigator monitors the health of each block throughout life and actively manages the programming conditions on the fly. Navigator will extract all the value available from NAND devices while improving data throughput.

Hence, this design maximizes the performance, longevity and cost for the specific applications running in the data center. The flexibility afforded by combining unique IP and NAND management into an architecture that utilizes an FPGA fabric allows for memory subsystems to be deployed alleviating data-center bottlenecks in a very cost effective, timely manner, without fear that the subsystem will itself degrade into another bottleneck over time.

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